Guest Lecture

ICT

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The SiLago Method: Next Generation VLSI Architecture and Design Methods

Abstract:

The VLSI community faces two challenges that we propose to address with the SiLago Method. The first problem is the unsustainably large engineering cost of VLSI design that is suffocating innovation and introduction of new product categories that requires orders of magnitude greater computational and silicon efficiencies that can only be achieved by custom hardware design. This recipe goes against the current state-of-the-practice software centric accelerator rich platform based design style that has not only failed to reduce the engineering cost but also delivers suboptimal designs and does not scale with technology trends.

As a solution, we propose raising the physical design platform from the present day boolean level standard cells to micro-architectural level SiLago (Silicon Large Grain Objects) blocks as the atomic physical design building blocks and introduce a grid based structured layout scheme as a new physical design discipline to compose arbitrary designs by abutting SiLago blocks to eliminate the logic and physical syntheses for the end user. We call this the SiLago method and show that it provides 2-3 orders more efficient synthesis from application level compared to the standard cell based commercial design flows with a modest loss in design quality.

The SiLago method also holds promise to solve the second problem of lowering the cost of making masks. This can be done because in the SiLago method, the mask becomes composable in terms of the component SiLago block masks. As there are finite number of SiLago block types that can have only a finite number of neighboring SiLago block types, it is possible to store as pre-determined patterns of the SiLago block types in a library that are corrected for all types of lithographic impairments. Masks for arbitrary SiLago designs can then be composed using these component SiLago block masks.

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Location: CD0404, Gußhausstraße 27-29, 4th floor

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