Abstract PhD Thesis

A Digital Metastability Model for VLSI Circuits

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This thesis develops a digital model for predicting failure rates caused by marginal triggering, so called metastability, of CMOS storage elements. To derive the underlying model, various storage elements are simulated in an industrial 90nm technology. The main characteristics of the responses of those elements are extracted from the results. The simulation findings are verified in hardware using measurements on an FPGA prototype. To achieve the required level of detail, the state of the art measurement circuits are not sufficient and are therefore extended. The main novelty for measuring D-flip flops is the possibility to perform a state-dependent response analysis and a significantly increased temporal resolution. Based on the case separation technique of the late transition detector for D-flip flops, a measurement infrastructure for Muller C-elements and RS-latches is developed as solutions for measuring asynchronous components using late transition detection were very basic before.

To verify the functionality of our newly developed metastability model, a comparison between a digital and an analogue simulation of a circuit comprising two D-latches is performed and the resulting failure rate plots demonstrate that the differences between the simulations are much smaller than the deviation caused by temperature, voltage and process variations.

Additionally an analysis on the propagation of short transient pulses in elastic pipelines, as caused by e.g. ionized particle hits, is performed. Therefore the constituting Muller C-elements are subjected to analogue simulation first and a method for containing non-digital output values within the element is derived. Based on those results, the elastic pipeline is simulated using different output stages for the Muller C-elements. The results indicate that the property of containing the propagation of unlatched pulses within the pipeline heavily depends on the used output stage.