Neural Models
For Monitoring and Control
with Applications in Automotive Domain

PhD THESIS
submitted in partial fulfillment of the requirements for the degree of
Doctor of Technical Sciences
within the
Vienna PhD School of Informatics
by

Dipl.Ing. Konstantin Selyunin
Registration Number 01228206

to the Faculty of Informatics
at the TU Wien
Advisor: Univ.Prof. Dipl.-Ing. Dr.rer.nat. Radu Grosu
Second advisor: Asst.-Prof. Dr. Ezio Bartocci
Industrial Co-advisor: Dr. Thang Nguyen

External reviewers:
Prof. Dr. Martin Leucker. Universität zu Lübeck, Germany.

Vienna, 9th October, 2017
Konstantin Selyunin
Radu Grosu
Abstract

Cyber-physical systems (CPS), which incorporate physical as well as computational components, are a grand challenge of academia and industry in terms of their development, verification, and maintenance. In order for CPS to serve their purpose and ultimately make human lives safer, easier, more enjoyable, and convenient, both academia and industry needs to develop new methods for control and monitoring of such systems. Neural models are a very promising and far looking direction for the design of CPS controllers and monitors. In this thesis we first show how neural models can be applied in CPS control to quantify the uncertainty of the system. We then present how digital spiking neural model, called TrueNorth, can be used in the runtime monitoring of temporal-logic specifications for mission-critical systems. In order to be able to deliver not only a qualitative verdict, but also to reason in a quantitative way, we propose an approach for modeling arithmetic-functions with spiking neurones, and implement neural monitors for (signal) temporal logic specifications based on circular convolution.

In the applied part of the thesis we demonstrate how runtime monitoring can speed up the verification and validation phases in automotive electronic development. We identify phases where runtime monitoring can facilitate both pre- and post-silicon verification and testing. To build runtime monitors that are capable of keeping up with the speed of the physical sensors, we developed an approach to convert formalized requirements to hardware monitors, which are then synthesized in an FPGA. The results of this work enable long-term requirements evaluation and foster reuse of the monitors from pre- to post-silicon verification phases using high-level synthesis. We illustrate our approach by formalizing, creating hardware monitors, and evaluating the results in the lab environment for electrical and timing requirements of the industrial SENT and SPC protocols.